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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/052,234	01/16/2002	Duc Chau	40013.003	9589

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EXAMINER	
GARCIA, JOANNIE A	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 04/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Advisory Action	Application No.	Applicant(s)	
	10/052,234	CHAU ET AL.	
	Examiner	Art Unit	
	Joannie A García	2823	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 05 April 2004 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE. Therefore, further action by the applicant is required to avoid abandonment of this application. A proper reply to a final rejection under 37 CFR 1.113 may only be either: (1) a timely filed amendment which places the application in condition for allowance; (2) a timely filed Notice of Appeal (with appeal fee); or (3) a timely filed Request for Continued Examination (RCE) in compliance with 37 CFR 1.114.

PERIOD FOR REPLY [check either a) or b)]

a) ☒ The period for reply expires 3 months from the mailing date of the final rejection.

b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.
ONLY CHECK THIS BOX WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

1. ☐ A Notice of Appeal was filed on _____. Appellant's Brief must be filed within the period set forth in 37 CFR 1.192(a), or any extension thereof (37 CFR 1.191(d)), to avoid dismissal of the appeal.

2. ☐ The proposed amendment(s) will not be entered because:

   (a) ☐ they raise new issues that would require further consideration and/or search (see NOTE below);

   (b) ☐ they raise the issue of new matter (see Note below);

   (c) ☐ they are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or

   (d) ☐ they present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: _____.

3. ☐ Applicant's reply has overcome the following rejection(s): _____.

4. ☒ Newly proposed or amended claim(s) 3,4,7-11 and 23 would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).

5. ☒ The a)☐ affidavit, b)☐ exhibit, or c)☒ request for reconsideration has been considered but does NOT place the application in condition for allowance because: See attachment.

6. ☐ The affidavit or exhibit will NOT be considered because it is not directed SOLELY to issues which were newly raised by the Examiner in the final rejection.

7. ☒ For purposes of Appeal, the proposed amendment(s) a)☐ will not be entered or b)☒ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.

   The status of the claim(s) is (or will be) as follows:

   Claim(s) allowed: 3,4,7-11 and 23.

   Claim(s) objected to: none.

   Claim(s) rejected: 1,2,5,6,12-22,24-31.

   Claim(s) withdrawn from consideration: _____.

8. ☐ The drawing correction filed on _____ is a)☐ approved or b)☐ disapproved by the Examiner.

9. ☐ Note the attached Information Disclosure Statement(s)(PTO-1449) Paper No(s). _____.

10. ☐ Other: _____

The 35 U.S.C. 112, second paragraph rejection for claim 14, has been withdrawn.

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 12-17, and 24, remain rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 12 and 24, recite the limitation "portion of the substrate not containing the nitride-containing layer" in lines 4-5, and 5-6, respectively. There is insufficient antecedent basis for this limitation in the claim.

Applicant argues that the claims are open to forming a nitride layer on the entire surface. However, the recited "providing a trench" step is contradictory to such a recitation. It must be made clear that the claims require providing a nitride containing layer on only a portion of the substrate upper surface, and that the trench is not formed in any particular remaining portion of the substrate.

Claims 6, 12, 16, 19, and 20, remain rejected under 35 U.S.C. 102(e) as being anticipated by Divakaruni et al (2002/014907 A1).

The rejection is maintained as stated in the Office Actions mailed 07-23-03, 01-29-04, and as stated below.

Applicant argues that Divakaruni et al fails to teach an oxide layer provided on the bottom and sidewalls of a trench, wherein said oxide layer is a high-quality gate oxide layer. However, the claims are not so limited. Furthermore, Divakaruni et al discloses providing a stacked silicon nitride/silicon oxide layer 20 on a bottom and sidewall of trench 16 (Figure 1C, and Paragraphs 0007, and 0008), and therefore, achieving formation of an oxide on a bottom of a trench.

Applicant argues that Divakaruni et al does not teach that the oxide layer of the stacked node dielectric 20 is formed on the bottom and sidewalls of trench 16. However, Divakaruni et al discloses that in the upper portion of the deep trench, the stacked node dielectric 20 serves as an etch stop layer (Paragraph 0007, lines 12-13), and one of ordinary skill in the art would have been drawn to employ the silicon nitride on top of the silicon oxide of stacked node dielectric 20, since silicon nitride, different from silicon oxide, is widely known to be used as etch stop material, and therefore, formation of an oxide layer on bottom and sidewalls of a trench would have been achieved. Furthermore, even if the silicon oxide would have been formed on top of the silicon nitride in stacked node dielectric 20, formation of an oxide layer on bottom and sidewalls of a trench would have been achieved, as well.

Divakaruni et al discloses a semiconductor device comprising providing a substrate 10 with an upper surface (Figure 1A), providing a nitride-containing layer 14 on a portion of the substrate upper surface (Figure 1A), providing a trench 16 in the substrate in a portion of the substrate not containing the nitride-containing layer (Figure 1B), providing an oxide layer 18 on a bottom and sidewall of the trench (Figure 1C, and Paragraph 0007, lines 1-3), providing a conductive layer 22 on a bottom and sidewall of the oxide layer (Figure 1D), the conductive

layer having an upper surface below the upper surface of the substrate (Figure 1D), providing by selective deposition a self-aligned isolation cap 50/28 on the conductive layer within the trench by using a combination of dielectric materials with different etching rates (Figure 2(d) and 4, and Paragraphs 0037 and 0038), and removing the nitride-containing layer (Figure 2(g)).

Claims 1, 2, 5, 12, 14, 15, 17, 18, 20, 21, 24, 25, and 27-31, remain rejected under 35 U.S.C. 102(b) as being anticipated by Baliga (U.S. Patent 5,998,833).

The rejection is maintained as stated in the Office Actions mailed 07-23-03, 01-29-04, and as stated below.

Applicant argues that Baliga does not teach forming an oxide layer on a bottom of a trench, and that it is improper to refer to the "empty space" above layers 24 and 26 in Figure 4F as a trench. However, the "empty space", as labeled by the applicant, is encompassed by the recitation of "trench", in view of the broadest reasonable interpretation, which is, for example, the class definitions for class 257, defining substrate as "the supporting material on or in which the components of an integrated circuit are fabricated or attached". It is not necessary for Baliga to label the "empty space 20" in Figure 4F as a trench. The fact that Baliga does not label "empty space 20" in Figure 4F as a trench, does not negate the examiner's interpretation of the scope of "trench". And the fact that Baliga labels 20 as a trench, does not prevent labeling the empty space 20 a trench, but instead provides the basis for labeling the "empty space 20" in Figure 4F as a trench, because both are grooves in a substrate. Therefore, formation of an oxide layer on a bottom of a trench would have been achieved.

Baliga discloses a semiconductor device comprising a substrate 10 with an upper surface 15a, the substrate having a trench therein (Figure 4A), source and channel regions 16/18 proximate a trench (Figure 4F), a gate oxide layer 28 on a bottom and sidewall of the trench (Figure 4G), a polysilicon conductive gate 30 on a bottom and sidewall of the gate oxide (Figure 4H, and Column 10, lines 9-12), the polysilicon conductive gate having an upper surface below the upper surface of the substrate (Figure 4H), a silicon oxide self-aligned isolation cap 32 on the polysilicon conductive gate within the trench (Figure 4I, and Column 10, lines 5-7).

Claim 13 remains rejected under 35 U.S.C. 103(a) as being unpatentable over Baliga as applied to claims 1, 2, 5, 12, 14, 15, 17, 18, 20, 21, 24, 25, and 27-31 above, and further in view of the following comments.

The rejection is maintained as stated in the Office Actions mailed 07-23-03, 01-29-04, and as stated above.

Claims 22 and 26 remain rejected under 35 U.S.C. 103(a) as being unpatentable over Baliga (U.S. Patent 5,998,833), in combination with Divakaruni et al (2002/0149047 A1).

The rejection is maintained as stated in the Office Actions mailed 07-23-03, 01-29-04, and as stated above.

Claims 3, 4, 7-11, and 23 are allowed.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group Receptionist whose telephone number is (703) 308-0956 until 2/4/04. See MPEP 203.08.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Joannie Adelle García whose telephone number is (571) 272-1861. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri, can be reached on (571) 272-1855. The fax number for this group is 703-872-9306 for before final submissions, 703-872-9306 for after final submissions and the customer service number for group 2800 is (703) 872-9317. Updates can be found at http://www.uspto.gov/web/info/2800.htm.

George Fourson
Primary Examiner
Art Unit 2823

JAG
January 9, 2004

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